Amendments to the Specification

Amendments are as follows:

Applicant amends paragraph beginning on page 2, line 18 as follows:

A2

In some portable systems, the transition between the two states occurs statically, for example, at reset or reboot. The ~~Geyserville™ the~~ state transition processor technology ~~of the Intel Corporation~~, on the other hand, is capable of dynamically transitioning between the two states, i.e., without a processor reset. The ~~Geyserville~~ technology is an improvement over the technology that changes the performance states statically because it achieves the transitions seamlessly and relatively rapidly without user intervention.

Amendments to the paragraph beginning on page 3, line 1 is as follows:

A3

Even ~~the dynamic Geyserville~~ this technology, however, may take more than 500 micro seconds to adjust the core supply voltage and the core clock frequency of the processor. This latency is the result of the processor being placed in the deep sleep mode (ACPI Specification C3 mode) during the entire transition. ACPI Specification stands for the Advanced Configuration and Power Interface Specification, Revision 2.0, published on July 27, 2000. Additional latency results to re-activate the system clock input to the processor to enable it to exit deep sleep following the transition.

Amendments to the paragraph beginning on page 3, line 9 are as follows:

A4

The high processor latency typically associated with transitioning states ~~Geyserville~~ is undesirable because it is wasted time that slows down the system operation.

Amendments to the paragraph beginning on page 5, line 2 is as follows:

A5

The present invention improves the ~~Geyserville~~ processor power state transition technology by reducing the processor latency associated with ~~Geyserville~~ the transition. Power dissipation of the processor is proportional to core clock frequency and to the square of core supply voltage. As the core clock frequency is reduced, the minimum required core supply voltage level is also reduced, thereby dramatically reducing the processor's power consumption. Depending on the power consumption desired of the system, the system may be set at one of the multiple performance states. For example, if the system is only powered by battery (such as, when the system is being used as a portable unit remotely without access to an external power supply), the system is placed in a low power state to conserve power. However, if the system is powered by an external power source (such as, an alternating current or AC outlet), the system is placed in a high performance state.

Amendments to the paragraph beginning on page 5, line 23 are as follows:

A6

Fig. 1 shows a transition graph to transition between the two states. In one embodiment, the transition, which may be performed by a controller formed of one or more layers (including, for example, software, firmware, and hardware), is performed in two different phases. In phase one, the core ~~supply~~

A6 end

~~voltage~~ clock frequency level is adjusted. In phase two, the core ~~clock frequency~~ supply voltage level is adjusted.

Amendments to the paragraph beginning on page 6, line 1 are as follows:

A7

During the low power to high performance transition~~, phase two follow phase one~~. The ~~the~~ core supply voltage level is elevated first such that it is at least the minimum voltage level required to support the elevated core clock frequency level of phase two.

Amendments to the paragraph beginning on page 6, line 8 are as follows:

A8

Performing phase 1 while the processor is in the active mode ~~is one key feature of the present invention because that~~ reduces the processor latency associated with ~~Geyserville~~ power state transition.

Amendments to the paragraph beginning on page 6, line 22 are as follows:

A9

~~Performing phase 2 while the processor is in the sleep mode is another key feature of the present invention.~~ Performing phase 2 in the sleep mode instead of the deep sleep mode (C3) reduces the latency to re-activate the system clock input to the processor after completing phase 2. In one embodiment of the present invention, phase 2 is performed in less than 5 microseconds.

Amendments to the paragraph beginning on page 7, line 4 are as follows:

A10

During the high performance to low power transition~~, phase 1 follows phase 2~~. The ~~the~~ processor clock frequency is reduced first such that when the processor supply voltage level is reduced later ~~on during phase 1~~, the reduced processor core voltage level is adequate to support it. ~~Phase 2 is performed in the same manner as with~~ With regards to the low power to high performance transition, ~~except that~~ the core frequency level is reduced instead of elevated.

~~Phase 1 is also performed in the same manner as with regards to the low power to high performance transition, except that the core voltage level is reduced instead of elevated.~~

AP end